PVP 14

Code: EC3T6, EE3T6

II B.Tech - I Semester – Regular Examinations – December 2015

SWITCHING THEORY AND LOGIC DESIGN

(Common for EEE, ECE)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) How do you perform subtraction using the 2's complement method?
   b) How do you obtain the dual of an expression?
   c) Can you call XOR gate as an inverter? Draw the inverter using XOR gate.
   d) What is a prime implicant chart?
   e) Why a binary -to-octal decoder is called a 1 to 8 decoder?
   f) How can a ROM device be considered as a combinational circuit?
   g) Which is the most versatile and most widely used of all the flip- flops?
   h) Differentiate between ring counter and Johnson counter?
   i) What are the capabilities and limitations of finite state machines?
   j) Compare the Moore and Mealy machines?
   k) What are the merits of Hamming code?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Using 2'S complements method perform. 6 M
   i) $(57)_{10}$- $(28)_{10}$
   ii) $(-75)_{10}$+$(26)_{10}$

   b) What is meant by parity checking? Explain the any two parity checking methods for Single bit error detection and correction with suitable examples. 10 M

3. a) Find the complement of the following expressions. 6 M
   i) $AB+A(B+C)+B^1(B+D)$
   ii) $A+B^1C(A+B+C^1)$

   b) Obtain the minimal SOP expression for
   $\sum m$ (2,3,5,7,9,11,12,13,14,15) and implement it using NAND logic. 10 M

4. a) Design of an even parity bit generator for a 4-bit input. 6 M

   b) Realize the following function using a PROM of size 8×3.
   $F1 = \sum m(0,4,7)$
   $F2 = \sum m(1,3,6)$
   $F3 = \sum m(1,2,4,6)$ 10 M

5. a) Convert a J-K Flip into 6 M
   i) SR Flip-flop
   ii) D Flip-flop

b) Design an asynchronous Modulo-6 Gray to binary code converter using T Flip flop. 10 M

6. A clocked sequential circuits with single input x and single output z produces an output z=1 Whenever the input x completes the sequence 1011 and overlapping is allowed.
   i) Obtain the state diagram.
   ii) Obtain its minimum state table and design the circuit with D flip-flop.

16 M